SUPER 286 BABY MAINBOARD 12 MHz ZERO WAIT

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SPECIFICATIONS

- * 6 or 12 MHz 80286 selectable by keyboard or by hardware switch, 80286-12 CPU.
- * 4MB high-speed memory standard
- 16MB expandable in the protected virtual address mode
- 2 sockets for PHOENIX, AWARD, ERSO or AMI BIOS (any BIOS fully compatible with IBMTM BIOS)
- * 8 I/O expansion slots
- * Socket for 80287 numeric processor
- * CMOS clock and calendar circuit
- * Battery on-board (easily serviced, easily replaced)
- * 6 custom chips set used to reduce total ICs
- * EMS control circuit
- * 24-bit addressing and 16-bit data pathing capabilities

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- * 16-level interrupt
- * 7-channel direct memory access (DMA)
- * 3-programmable timers
- Speaker/keyboard connector
- * StandardAT[™] power supply connector
- * Small AT[™] dimensions
- * High temperature burned-in
- * 0-wait state or 1-wait state selectable

How to Set Up Your 286 Motherboard

A. BIOS ROM

- 1. BIOS ROM (Lo) is inserted into ROM1.
- 2. BIOS ROM (Hi) is inserted into ROM 2.



Figure 1

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- 3. When ROM type 27128 is used, DIP switch -5 is set to ON.
- 4. When ROM type 27256 is used, DIP switch -5 is set to OFF



Figure 2



B. KEYBOARD BIOS

1. 8742 with keyboard BIOS programmed in it is inserted into the location marked "8742".



- 2. When an AWARD type keyboard BIOS (switchable by using port 22) is used, JP3 is set to CLOSE,
- 3. When a PHOENIX type keyboard BIOS (switchable by using Port 15) is used, JP1 is set to CLOSE



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- C. DRAM
 - 1. A total of 8 (0-7) modes are available depending on memory sizes, for insertion of DRAMs. The figures below show the methods of DRAM insertion. When 4164 or 41256 DRAM is used, the DRAM is inserted into the 16-pin side. When 421000 DRAM is used, it is inserted into the 18-pin side.





Figure 5

Figure 6

MODE SETTINGS



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Figure 7



2. MODE 0

A total of 18 DRAMs(41256-8) are inserted onto BANK0. The DIP switches -6, -7, -8 are each set to ON. In MODE 0, the memory location is 00000 - 7FFFFH and the memory size is 512KB.

3. MODE 1

A total of 18 DRAMs (41256-8) are inserted onto BANK 0, and a total of 18 DRAMs (4164-8) are inserted onto BANK 1. The DIP switches -6, -7, and -8 are set to ON, ON, and OFF respectively. In MODE 1, the memory location is 00000 - 9FFFFH and the system memory size is 640KB.

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4. MODE 2

A total of 18 DRAMs(41256-8) are inserted onto BANK 0, and a total of 18 DRAMs(41256-8) are inserted onto BANK 1. The DIP switches -6, -7, and -8 are set to ON, OFF and ON respectively. In MODE 2, the memory locations are 00000 - 9FFFFH and 100000H - 15FFFFH. System memory size is 640KB and expansion memory size is 384KB.

5. MODE 3

A total of 18 DRAMs (41256-8) are inserted onto BANK 0 and a total of 18 DRAMs (41256-8) are inserted onto BANK 1. The DIP switches -6, -7, and -8 are set to ON, OFF and OFF respectively. In MODE 3, the memory location is 00000 - 9FFFFH and the system memory size is 640KB + EMS (384KB). The EMS (384KB) memory can be used as an EXPAND memory with a capacity of 16KB x 24 pages, by using a SUNTAC EMS driver program.

6. MODE 4

A total of 18 DRAMs(421000-8) are inserted into BANK 0. The DIP switches -6, -7, and -8 are set to OFF, ON and ON respectively. In MODE 4, the memory locations are 00000 - 9FFFFH

and 100000H - 25FFFFH and the system memory size is 640KB + 1,408KB.

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7. MODE 5

A total of 18 DRAMs(421000-8) are inserted onto BANK 0. The DIP switches -6, -7 and -8 are set to OFF, ON, and OFF respectively. In MODE 5, the memory location is 00000 - 9FFFFH; the system memory size is 640KB + EMS (1,408KB). The EMS (1,408KB) memory can be used as an EXPAND memory with a capacity of 16KB x 88 pages, by using a SUNTAC EMS driver program.

8. MODE 6

A total of 18 DRAMs (421000-8) are inserted onto BANK 0 and a total of 18 DRAMs (421000-8) are inserted onto BANK 1. The DIP switches -6, -7 and -8 are set to OFF, OFF and ON respectively. In MODE 6, the memory locations are 00000 - 9FFFFH and 100000H - 45FFFFH; the system memory size is 640KB + 3,456KB.

9. MODE 7

A total of 18 DRAMs(421000-8) are inserted onto BANK 0 and a total of 18 DRAMs(421000-8) are inserted onto BANK 1. The DIP switches -6, -7 and -8 are set to OFF, OFF and OFF respectively. In MODE 7, the memory location is 00000 - 9FFFFH and the system memory size is 640KB + EMS (3,456KB). The EMS (3,456KB) memory can be used as an EXPAND memory with a capacity of 16KB x 216 pages by using a

a capacity of 16KB x 216 pages, by using a SUNTAC EMS driver program.

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D. MONITOR TYPE

- 1. When a color monitor is used, DIP switch -2 is set to ON.
- 2. When a monochrome monitor is used, DIP switch -2 is set to OFF.



Figure 9



E. CLOCK SPEED SWITCHING

- When switching speeds externally: 1. A mechanical switch is installed onto JP7, JP7 in the OPEN state provides Low speed, when CLOSED, it provides High speed.
- When JP7 is OPEN, the clock speed can be 2. switched by using the keyboard. When using AWARD BIOS, keys CTRL, ALT and (minus) are pressed simultaneously to switch to High speed. Keys CTRL, ALT and + (plus) are pressed simultaneously to switch to Low speed.
- If the power is turned on while JP7 is OPEN, it 3. will turn to Low speed. If JP7 is CLOSED; it will invalidate the keyboard operation and will switch to High speed at all times.
- When using PHOENIX BIOS, keys CTRL ALT 4. are pressed simultaneously to switch and speeds.



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F. EMS PORT ADDRESS

- 1. When using 098 - 09FH as the EMS Port Address, DIP switch -4 is set to OFF. The SUNTAC EMS driver program setting is used at this point.
- 2. When using 0E8 0EFH as the EMS Port Address. DIP switch -4 is set to ON. The SUNTAC EMS driver program setting is used at this point.





G. RESET SWITCH



STATE SELECTION

A mechanical switch is installed onto JP5. When JP5 is OPEN, the setting will be one wait state. When JP5 is CLOSED, the setting will be zero wait state.



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INSTALLATION

Peripherals required:

- 1) 286 Motherboard
- 2) IBMATTM power supply or compatible equivalent
- 3) IBMTM monochrone/graphics display board, color card, EGA card or compatible equivalent
- 4) IBMTM keyboard or compatible equivalent
- 5) Monochrome, color, or EGA monitor

Procedures:

- 1) Connect power supply connectors to P8 as marked.
- 2) Plug in keyboard connector to the keyboard receptical (J22) at the back.
- 3) Install monochrome or color graphic display board in expansion slot 1 or 7.
- 4) Select monochrome or color at DIP switch -2.
- 5) Connect monitor cable to the display board.6) Make sure "LOW BYTE" or "EVEN BYTE" BIOS is on IC23.
- 7) Make sure "HIGH BYTE" or "ODD BYTE" BIOS is on IC33.
- 8) Set the RAM size as follows by DSP1: #6-8.

#8	#7	#6	MODE	SIZE		
ON	ON	ON	0	512KB		
OFF	ON	ON	1	640KB		
ON	OFF	ON	2	640KB	+	384KB
OFF	OFF	ON	3	• 640KB	+	EMS (384KB)
ON	ON	OFF	4	640KB	+	1408KB
OFF	ON	OFF	5	640KB	+	EMS (1048KB)
ON	OFF	OFF	6	640KB	+	3456KB
OFF	OFF	OFF	7	640KB	+	EMS (3456KB)

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- 9) For those which have the IBM PC/AT[™] chasis or compatible equivalent, plug in the speaker connector to SP, and the "Power LED and EXT LOCK" connector to J20 at the front, and the "TURBO LED" connector to JP8.
- 10) Turn on the monitor.
- 11) Turn on the power supply.



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EMS DRIVER SET-UP

- 1. Boot your PCTM system by using DOSTM and the system will prompt you with A > .
- 2. Copy the SEMS.SYS file onto your DOSTM diskette.
- 3. Type:

COPY CON CONFIG.SYS < Return > DEVICE=SEMS.SYS /M:xxx /P:xxxx /I:xxx < Return > ^Z < Return >

- where M:xxx = System memory size, default is 640KB.
 - P:xxxx = EMS Physical page segment address, default automatic.
 - I:xxx = EMS Port address E8H or 98H.

The screen will display as follows:

1 File(s) copied

A>

4. Reboot your system. The following screen will appear:

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5. You can run RAMBANK SOFTWARE like VD.SYS, PB.COM, or RAMTEST.

Example:

If 384K has been set as the virtual disk, type in the command line as follows:

COPY CON CONFIG.SYS <Enter> DEVICE=SEMS.SYS <Enter> DEVICE=VD.SYS /384/ <Enter> ^Z <Enter>

- Note: 1. The EMS software supports SEMS, SEMS4, SEMS5.
 - If you have VGA & ARCNET in your system, you probably need to set DEVICE-SEMS5.SYS/ P:CCOO/.



INSTRUCTION FOR EMS DRIVER PREPARATION

1. After the power is turned on, and before DRAM begins refreshing, an initial value needs to be written into EMS Register R0. (This writing should done within BIOS ROM.)

Initial values (1) Write 9DH when I/O port address is E8H.

- (2) Write 93H when I/O port address is 98H.
- When the data has been written into EMS Registers R0-R7, Bit 7 in R0 has to be read in order to confirm whether the Register contents have been transferred from DADR to HADA.
 - (1) When Bit 7 in R0 is 1, the transfer has yet to be achieved.
 - (2) When Bit 7 in R0 is 0, the transfer has been achieved.
- 3. The system memory size in the EMS Register should not be set at any value larger than 640KB (A0H).
- 4. The segment start address in EMS Register R3 should not be set at any value smaller than the system memory size (R2).

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5. When setting the page numbers of banks 0-3 in EMS Registers R4-R7, the numbers should correspond to the page numbers counted, by 16KB units, from the DRAM address 0000 : 000H.

Example:

When EMS has a system memory size of 640 KB and the usable page head is to be set:

640 - 16 = 40 (28H)

Therefore, 28H is set as the page head.

Incidentally, a physical page can be released by setting its corresponding bank at 0.

- 6. The banks 0-3 in EMS Registers R4-R7 are always in correspondence to physical pages 0-3
- 7. When the system memory size is 1MB (as shown in the Memory Address Setting 3 on page 28) the setting of EMS page No. at 40H will result in the production of an image from the memory's 0000 : 0000H.
- EMS maximum pages Nos. are 216 pages at 4MB. The memory size that can be used with DOS[™] is 640KB.



EMS INTERFACE

EMS Port Address

EMS98/E8	Location	Description
"L"	E8H	Access to 80287 is impossible at E8-EFH.
"H"	98H	Access to 74LS612 is impossible at 98-9FH.

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EMS Registers

		D7	D6	D5	D4	D3	D2	D1	DO	Description
	Variable port	T/R	Variable port address.						T/R flag Read	
RO	address. Transfer flag. (Read) RO Read enable (Write)	flag	A9	A8	A7	A6	A5	Α4	АЗ	1:Transfer yet to be done 0:Transfer done Write 1:Read possible 0:Read impossible
R1	Reserved									
R2	System mem- ory size	A19	A18	A17	A16	A15	A14	fixe	d 0	Read impossible (A0H 00000-9FFFFH)
R3	Segment start address	A19	A18	A17	A16	A15	A14	fixe	d 0	Read impossible (COH:segmentC000H)
R4	Bank 0	P7	P6	P5	P4	P3	P2	P1	P0	Read impossible
R5	Bank 1	P17	P16	P15	P14	P13	P12	P11	P10	Read impossible
R6	Bank 2	P27	P26	P25	P24	P23	P22	P21	P20	Read impossible
R7	Bank 3	P37	P36	P35	P34	P33	P32	P31	P30	Read impossible



CONNECTOR PINOUTS

1. POWER SUPPLY CONNECTOR (P8)

DESCRIPTION
POWER GOOD
+ 5V DC
+ 12V DC
-12V DC
GROUND
GROUND
GROUND
GROUND
-5V DC
+5V DC
+5V DC
+ 5V DC

2. SPEAKER CONNECTOR (J19)

PIN	DESCRIPTION
1	SPEAKER DATA OUT
2	KEY
3	GROUND
4	+5V DC

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3. KEYBOARD SWITCH & LED CONNECTOR (J20)

PIN	DESCRIPTION
1	LED POWER
2	KEY
3	GROUND
4	KEYBOARD INHIBITOR
5	GROUND

4. KEYBOARD CONNECTOR (J22)

PIN	DESCRIPTION
1	KEYBOARD CLOCK
2	KEYBOARD DATA
3	SPARE
4	KEYBOARD GROUND
5	+5V DC



5. RESET CONNECTOR (JP6)

PIN	DESCRIPTION
1	RESET IN
2	GROUND



6. HIGH SPEED LED CONNECTOR(TUBLED)

PIN	DESCRIPTION
1	+ ANODE
2	- CATHODE

NOTES:

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- 1) XTAL SET 20MHz = LED ON
- 2) XTAL SET 12MHz = LED OFF



I/O CHANNELS

The following figures show the location and the numbering of the I/O channel connectors. These connectors consist of eight pin and six 36-pin edge connector sockets.

REAR PANEL

-MEM CS16	ID1	C1I	SBHE
-I/O CS16	ID2	C2I	
IR 10		C3I	LA22
IR 11	ID4	C4I	LA21
IR 12	ID5	C5I	
IR 15		C6I	
IR 14		C7I	
-DACK 0		C8I	
DRA 0		С9І	MEMR
-DACK 5	ID10	C10I	
DRQ 5	ID11	C11I	
-DACK 6	ID12	C12I	SD09
DRQ 6		C13I	
-DACK 7	ID14	C14I	
DRQ 7	ID15	C15I	
+5V	ID16	C16I	
-MASTER	ID17	C17I	
GND	ID18	C18I	SD15

I/O CHANNEL PIN NUMBERING



REAR PANEL

GNDIB1RESET DRVIB2 $+5V$ IB3IR9IB4 $-5V$ IB5DRQIB6 $-12V$ IB7OWSIB8 $+12V$ IB9GNDIB10 $-S$ MEMWIB11 $-S$ MEMWIB11 $-S$ MEMRIB12 $-IOW$ IB13 $-IOR$ IB14 $-DACK$ 3IB15DRQ 3IB16 $-DACK$ 1IB17DRQ 1IB18 $-REFRESH$ IB19SYSCLKIB20IR 7IB21IR 6IB22IR 5IB23IR 4IB24IR 3IB25 $-DACK$ 2IB26 T/C IB27BALEIB28 $+5V$ IB29OSCIB30GNDIB31	CND	ID 1
+5VIB3IR9IB4 $-5V$ IB5DRQIB6 $-12V$ IB7OWSIB8 $+12V$ IB9GNDIB10 $-S$ MEMWIB11 $-S$ $-S$ MEMWIB12 $-IOW$ IB13 $-IOR$ IB14 $-DACK$ 3IB15DRQ 3DRQ 1IB18 $-REFRESH$ IB19SYSCLKIB20IR 7IB21IR 6IB22IR 5IB23IR 4IB24IR 3IB25 $-DACK$ 2IB26T/CIB27BALEIB28 $+5V$ IB29OSCIB30	GND	IBI
IR9 IB4 -5V IB5 DRQ IB6 -12V IB7 OWS IB8 + 12V IB9 GND IB10 -S MEMW -S MEMW -IOW IB12 -IOW IB13 -IOR IB14 -DACK 3 IB15 DRQ 3 IB16 -DACK 1 IB17 DRQ 1 IB18 -REFRESH IB19 SYSCLK IB20 IR 7 IB21 IR 6 IB22 IR 5 IB23 IR 4 IB24 IR 3 IB25 -DACK 2 IB26 T/C IB27 BALE IB28 + 5V IB29 OSC IB30		
-5V IB5 DRQ IB6 $-12V$ IB7 OWS IB8 $+ 12V$ IB9 GND IB10 $-S$ MEMW $-S$ MEMW $-S$ MEMW $-S$ MEMR $-IOR$ IB13 $-IOR$ $-IB14$ $-DACK$ 3 $-DACK$ 1 $-S$ IB20 IR 7 $IB21$ IR IR 5 $-DACK$ 2 IR 5 $-DACK$ 2 $-DACK$ 2 $-DACK$ 2		
-5V IB5 DRQ IB6 $-12V$ IB7 OWS IB8 $+ 12V$ IB9 GND IB10 $-S$ MEMW $-S$ MEMW $-S$ MEMW $-S$ MEMR $-IOR$ IB13 $-IOR$ $-IB14$ $-DACK$ 3 $-DACK$ 1 $-S$ IB20 IR 7 $IB21$ IR IR 5 $-DACK$ 2 IR 5 $-DACK$ 2 $-DACK$ 2 $-DACK$ 2	IR9	IB4
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	-5V	
-12VIB7OWSIB8 $+12V$ IB9GNDIB10 $-S$ MEMWIB11 $-S$ MEMRIB12 $-IOW$ IB13 $-IOW$ IB13 $-IOR$ IB14 $-DACK$ 3IB15DRQ 3DRQ 3IB16 $-DACK$ 1DRQ 1IB18 $-REFRESH$ IB19SYSCLKIB20IR 7IB21IR 6IB22IR 5IB23IR 4IB24IR 3IB25 $-DACK$ 2IB26T/CT/CIB27BALEIB28 $+ 5V$ IB29OSCIB30	DRO	IB6
OwsIB8 $+ 12V$ IB9GNDIB10-SMEMWIB11-SMEMRIB12-IOWIB13-IORIB13-IORIB14-DACK 3IB15DRQ 3IB16-DACK 1IB17DRQ 1IB18-REFRESHIB19SYSCLKIB20IR 7IB21IR 6IB22IR 5IB23IR 4IB24IR 3IB25-DACK 2IB26T/CIB27BALEIB28+ 5VIB29OSCIB30	-12V	IB7
+ 12VIB9GNDIB10-SMEMWIB11-SMEMRIB12-IOWIB13-IORIB13-IORIB14-DACK 3IB15DRQ 3IB16-DACK 1IB17DRQ 1IB18-REFRESHIB19SYSCLKIB20IR 7IB21IR 6IB22IR 5IB23IR 4IB24IR 3IB25-DACK 2IB26T/CIB27BALEIB28+ 5VIB29OSCIB30	OWS	IB8
$\begin{array}{llllllllllllllllllllllllllllllllllll$	+12V	IR9
-S MEMW IB11 -S MEMR IB12 -IOW IB13 -IOR IB13 -IOR IB14 -DACK 3 IB15 DRQ 3 IB16 -DACK 1 IB17 DRQ 1 IB18 -REFRESH IB19 SYSCLK IB20 IR 7 IB21 IR 6 IB22 IR 5 IB23 IR 4 IB24 IR 3 IB25 -DACK 2 IB26 T/C IB27 BALE IB28 + 5V IB29 OSC IB30		
-S MEMR IB12 -IOW IB13 -IOR IB14 -DACK 3 IB15 DRQ 3 IB16 -DACK 1 IB17 DRQ 1 IB18 -REFRESH IB19 SYSCLK IB20 IR 7 IB21 IR 6 IB22 IR 5 IB23 IR 4 IB24 IR 3 IB25 -DACK 2 IB26 T/C IB27 BALE IB28 + 5V IB29 OSC IB30	-S MEMW	IB 11
-IOW $IB13$ $-IOR$ $IB14$ $-DACK$ 3 DRQ 3 $IB15$ DRQ 3 $IB16$ $-DACK$ 1 $IB17$ DRQ 1 $IB18$ $-REFRESH$ $IB19$ $SYSCLK$ $IB20$ IR IR 7 $IB21$ IR 6 $IB22$ IR 5 $IB23$ IR 4 $IB24$ IR 3 $IB25$ $-DACK$ 2 $IB26$ T/C $IB27$ $BALE$ $IB29$ OSC $IB30$	-S MEMR	\mathbf{B}_{12}
-IORIB14-DACK 3IB15DRQ 3IB16-DACK 1IB17DRQ 1IB18-REFRESHIB19SYSCLKIB20IR 7IB21IR 6IB22IR 5IB23IR 4IB24IR 3IB25-DACK 2IB26T/CIB27BALEIB28+ 5VIB29OSCIB30	-IOW	IR13
-DACK 1 IB10 $-DACK$ 1 IB17 DRQ 1 IB18 $-REFRESH$ IB19 $SYSCLK$ IB20 IR 7 IB21 IR 6 IB22 IR 5 IB23 IR 4 IB24 IR 3 IB25 $-DACK$ 2 IB26 T/C IB27 BALE ALE IB28 + 5V OSC IB30	-IOR	IB 14
-DACK 1 IB10 $-DACK$ 1 IB17 DRQ 1 IB18 $-REFRESH$ IB19 $SYSCLK$ IB20 IR 7 IB21 IR 6 IB22 IR 5 IB23 IR 4 IB24 IR 3 IB25 $-DACK$ 2 IB26 T/C IB27 BALE ALE IB28 + 5V OSC IB30	-DACK 3	IB15
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	DRO 3	IB 16
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	-DACK 1	B 17
-REFRESH IB19 SYSCLK IB20 IR 7 IB21 IR 6 IB22 IR 5 IB23 IR 4 IB24 IR 3 IB25 -DACK 2 IB26 T/C IB27 BALE IB28 + 5V IB29 OSC IB30	DRO 1	IR18
SYSCLK IB20 IR 7 IB21 IR 6 IB22 IR 5 IB23 IR 5 IB23 IR 4 IB24 IR 3 IB25 -DACK 2 IB26 T/C IB27 BALE IB28 + 5V IB29 OSC IB30	REFRESH	IR 10
IR 7 IB21 IR 6 IB22 IR 5 IB23 IR 5 IB23 IR 4 IB24 IR 3 IB25 -DACK 2 IB26 T/C IB27 BALE + 5V IB29 OSC OSC IB30	SVSCLK	IB20
IR 6 IB22 IR 5 IB23 IR 4 IB24 IR 3 IB25 -DACK 2 IB26 T/C IB27 BALE BALE IB28 + 5V OSC IB30		
IR 5 IB23 IR 4 IB24 IR 3 IB25 -DACK 2 IB26 T/C IB27 BALE IB28 + 5V IB29 OSC IB30		
IR 3 IB25 -DACK 2 IB26 T/C IB27 IB27 BALE IB28 +5V IB29 OSC IB30 IB30		
IR 3 IB25 -DACK 2 IB26 T/C IB27 IB27 BALE IB28 +5V IB29 OSC IB30 IB30	IN 5 ID A	1023
BALE IB28 +5V IB29 OSC IB30	IN 4 ID 2	ID24
BALE IB28 +5V IB29 OSC IB30	IK 5 DACK 2	IB25
BALE IB28 +5V IB29 OSC IB30	-DACK 2	IB20
+5V1B29 OSCIB30		1B2/
+5V1B29 OSCIB30	BALE	IB28
GND IB30 IB31	+ 3 V	IB77
GND IB31	OSC	IB30
	GND	IB31

A1I -I/O CH CK
A2I SD7
A3I SD6
A4I SD5
A5I SD4
A6I SD3
A7L SD2
A8LSD1
A9LSD0
A10I -I/O CH RDY
A11I AEN
A12I SA19
A13I SA18
A14I SA17
A15I SA16
A16I SA15
A17I SA14
A18I SA13
A19I SA12
A20I SA11
A21I SA10
-A221SA9
A23I SA8
A241SA7
A25I SA6
A26I SA5
A271 SA4
A281 SA3
A291SA2
A301SA1
A31I SA0

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I/O CHANNEL PIN NUMBERING



SYSTEM BLOCK DIAGRAM



MEMORY ADDRESS

DRAM

NO	DIP Switch setting			Memory type		Memory size	Memory
	S6	S7	S8	BANK1	BANKO	Wernory Size	Location
0	ON	ON	ON	NONE	256Kbits	512KB	0-7FFFF
1	ON	ON	OFF	64Kbits	256Kbits	640KB	0-9FFFF
2	ON	OFF	ON	256Kbits	256Kbits	640KB + 384KB	0-9FFFF 100000-15FFFF
3	ON	OFF	OFF	256Kbits	256Kbits	640KB+EMS (16KB X 24pages)	0-9FFFF
4	OFF	ON	ON	NONE	1Mbits	640KB + 1408KB	0-9FFFF 100000-25FFFF
5	OFF	ON	OFF	NONE	1Mbits	640KB+EMS (16KB X 88pages ¹	0-9FFFF
6	OFF	OFF	ON	1 Mbits	1Mbits	640KB + 3456KB	0-9FFFF 100000-45FFFF
7	OFF	OFF	OFF	1Mbits	1 Mbits	640KB+EMS (16KB X 216pages)	0-9FFFF



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