Technical Information Manual

S78H-5142-00

PC 100 (Type 6260) and PC 300 (Type 6560)

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Note

Before using this information and the product it supports, be sure to read the general information under Appendix B, “Notices and Trademarks” on page 43.

First Edition (August 1996)

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Preface

This *Technical Information Manual* provides information about the IBM PC 100 (Type 6260) and the IBM PC 300 (Type 6560). It is intended for developers who want to provide hardware and software products to operate with these IBM computers and provides a more in-depth view of how the computers work. Users of this publication should have an understanding of computer architecture and programming concepts.

Related Publications

In addition to this manual, the following IBM publications provide information related to the operation of the PC 100 and PC 300. To order publications in the U.S. and Puerto Rico, call 1-800-879-2755. In other countries, contact an IBM reseller or an IBM marketing representative.

- *Using Your Personal Computer – PC 100*[1]
- *Hardware Maintenance Manual – PC 100*[1]
- *Using Your Personal Computer – PC 300*
- *Installing Options in Your Personal Computer – PC 300*
- *Understanding Your Personal Computer – PC 300*
- *Hardware Maintenance Manual – PC 300*

Manual Style

Attention: The term *reserved* describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

In this manual, signals are represented in a small, all-capital-letter format (-ACK). A minus sign in front of the signal indicates that the signal is active low. No sign in front of the signal indicates that the signal is active high.

In this manual, use of the letter “h” indicates a hexadecimal number. Also, when numerical modifiers such as “K”, “M” and “G“ are used, they typically indicate powers of 2, not powers of 10 (unless expressing hard disk storage capacity). For example, 1 KB equals 1 024 bytes (2^{10}), 1 MB equals 1 048 576 bytes (2^{20}), and 1 GB equals 1 073 741 824 bytes (2^{30}).

When expressing storage capacity, MB equals 1 000 KB (1 024 000). The value is determined by counting the number of sectors and assuming that every two sectors equals 1 KB.

The actual storage capacity available to the user can vary, depending on the operating system and other system requirements.

[1] Not available in the U.S. and Puerto Rico.

Chapter 1. System Description

Personal Computer Description

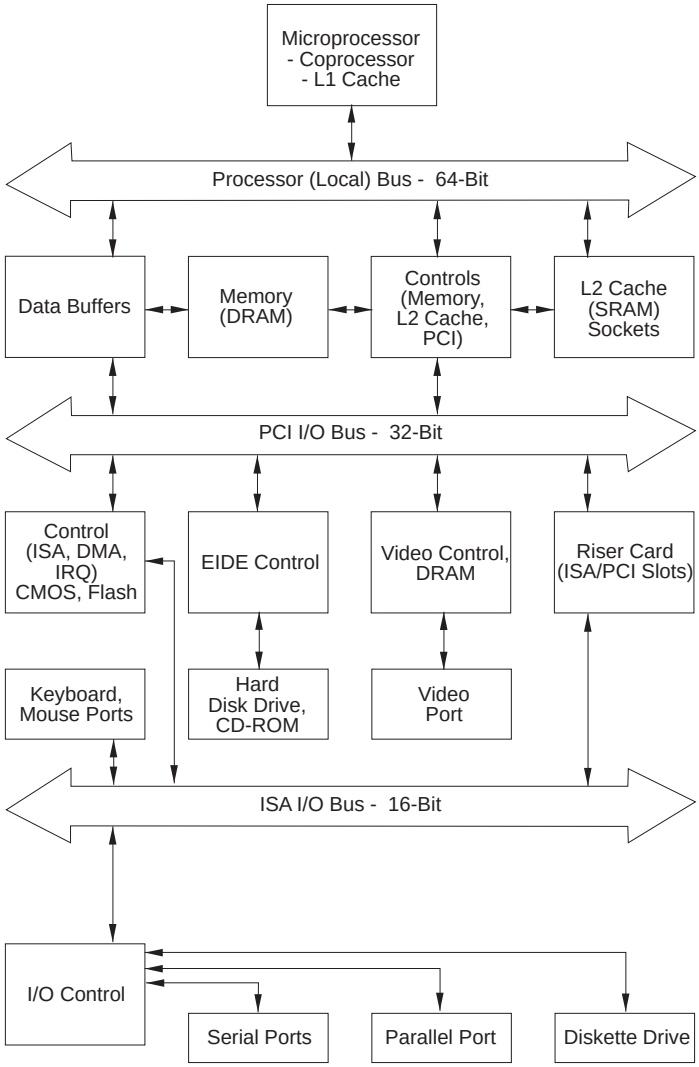
The IBM PC 100 (Type 6260) and PC 300 (Type 6560) are versatile products designed to provide state-of-the-art computing power with room for growth in the future. The two computer models are similar in design, utilizing the same cover, frame assembly, and system board. They differ in the type of BIOS resident and in the mix of standard features.

The major features of the PC 100 and PC 300 are:

- Intel Pentium microprocessor
- Up to 128 MB of system memory
- Cirrus GD5436 video subsystem
- 1 MB of video memory with sockets for additional 1 MB
- Industry-standard compatibility
- ISA/PCI I/O-bus compatibility
- ISA/PCI expansion slots
- Enhanced EIDE hard disk drive
- Bus master-capable EIDE controller
- Two 16550-UART serial ports (serial A and serial B)
- L2 cache sockets for pluggable SRAMS (256 KB)
- Support for advanced power management
- EnergyStar compliant
- Support for Plug and Play adapters and monitors
- Security features
- System unit size
  - Four expansion slots
  - Four drive bays

Note: Several model variations are available for both the PC 100 and the PC 300.

System Overview



System Features

The following figure lists the devices and features of the PC 100 and PC 300 system board. It also includes some of the options that may be added to these computers.

Figure 1 (Page 1 of 2). System Board Devices, Features, and Options

Device	Features
Microprocessor	Intel Pentium (75/100/120/133 MHz)[2] • 32-bit address bus, 64-bit data bus • 8 KB internal (L1) write-through code cache • 8 KB internal (L1) write-back data cache • Superscalar architecture (two execution units) • Math coprocessor function included in the Pentium Microprocessor is upgradable for future Intel microprocessor technology
External Cache (L2)	DIP sockets for user-installable data/tag RAMs 256 KB asynchronous write-back unified (code and data)
Video Subsystem	Cirrus Logic GD5436 SVGA video controller • Plug and Play monitor support (DDC2) • Advanced Power Management • Local peripheral bus (LPB) interface • 64-bit data path width on PCI bus • Integrated DAC • 64-bit graphics accelerator 1 MB of 70 ns FP DRAM • Fast Page Mode DRAM • Sockets for additional 1 MB
Bus Architecture	ISA/PCI-bus-compatible I/O expansion slots Synchronous 25/30/33 MHz PCI bus 50/60/66 MHz processor bus Integrated L2 cache controller
Flash ROM Subsystem	256 KB flash ROM for POST/BIOS
RAM Subsystem	8 MB standard DRAM, upgradable to 128 MB 70-ns fast page (FP) or 60-ns extended data output (EDO), non-parity, dynamic random access memory (DRAM) Four 72-pin SIMM sockets in two banks • SIMMs (4 MB, 8 MB, 16 MB, or 32 MB) • Matched pairs required in each bank
CMOS RAM Subsystem	128-byte CMOS RAM with real-time clock, calendar, and battery
ISA/PCI Bridge	ISA/PCI interface PCI bus-master EIDE interface ISA-compatible interrupt controller ISA-compatible DMA controller
DMA Controller	Seven AT-compatible DMA channels • Four 8-bit channels • Three 16-bit channels
Interrupt Controller	15 levels of system interrupts • AT bus interrupts are edge triggered • PCI bus interrupts are level sensitive
System Timers	Channel 0–System timer Channel 1–Refresh generation Channel 2–Tone generation for speaker
Audio Subsystem	On-board Piezo electric beeper

[2] MHz denotes internal clock speed of the microprocessor only; other factors might also affect application performance.

Figure 1 (Page 2 of 2). System Board Devices, Features, and Options

Device	Features
Diskette Drive Controller	Controller supports up to two internal diskette drives • A 3.5-in. diskette drive (1.44 MB) is standard • A 5.25-in. diskette drive (1.2 MB) is optional • A second 3.5-in. diskette drive (1.44 MB) is optional and requires a 3.5-in. conversion kit for a 5.25-in. bay FIFO operations
Keyboard/Auxiliary-Device Controller	101-key or 104-key keyboard Keyboard connector Auxiliary-device (mouse) connector
Parallel Port Controller	One ECP/EPP parallel port Supports standard I/O mode, extended capabilities port (ECP) mode, and enhanced parallel port (EPP) mode
Serial Port Controller	Two 16550-UART serial ports (Serial A and B)
Hard Disk Drive Controller	Controller supports four EIDE devices PCI bus-master EIDE interface • Two PCI bus-master channels • One channel for each EIDE connector (primary and secondary) • SCSI hard disk drives require a PCI SCSI adapter
Power	145 watt (115/230 V ac, 50/60 Hz) power supply Built-in overload and surge protection Advanced Power Management
Security	Power-on password Administrator password Startup sequence control Unattended Start mode Diskette I/O control Hard disk I/O control

System Board

The following is a diagram of the PC 100 and PC 300 system board. Note that the system board for these computers might differ slightly from the one shown. A diagram of the system board, including switch and jumper settings, is provided on the underside of the computer cover.

1	J3 Power connector (5 V)
2	JP11 Flash jumper
3	JP21 FDD write protect
4	JP4 PS/2 mouse enable/disable
5	J5 Diskette drive connector
6	JP23 HDD detect
7	J8 Primary IDE connector
8	J7 Secondary IDE connector
9	Battery
10	J9 Password jumper (CMOS clear)
11	L2 cache memory sockets
12	JP22 Burst mode
13	JP19 CPU voltage
14	Processor socket
15a	J12 Power LED connector
15b	J12 Hard disk drive LED connector
16	J13 CPU fan connector
17	JP17 CPU clock
18	SIMM connector 1 - Bank 1
19	SIMM connector 2 - Bank 1
20	SIMM connector 3 - Bank 0
21	SIMM connector 4 - Bank 0
22	Tag RAM socket
23	J6 Video feature connector
24	JP13 Cache memory size
25	JP14 CPU bus clock
26	JP3 On-board VGA
27	P4 Monitor (display) port
28	P1 Parallel port[3]
29	Video memory sockets
30	P2 Serial (B) port
31	PCI/ISA riser connector
32	P3 Serial (A) port
33	J2 Auxiliary device (mouse) port
34	J1 Keyboard port

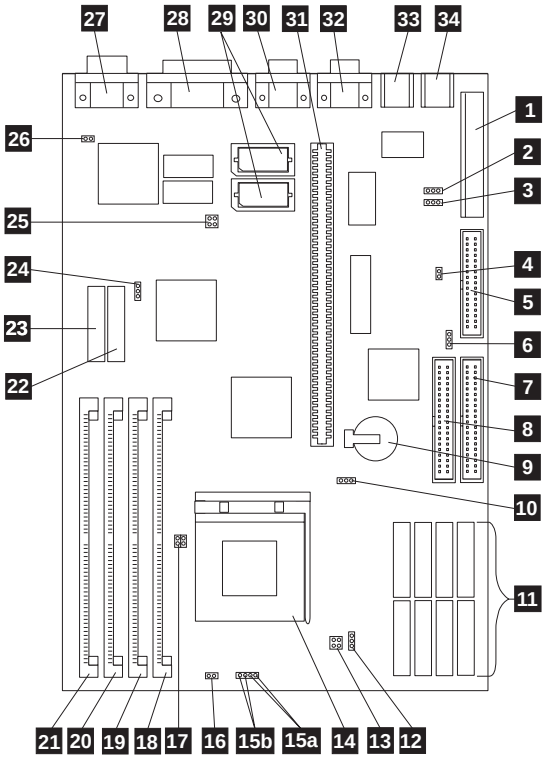


Figure 2. System Board Diagram

[3] Extended capabilities port/enhanced parallel port (ECP/EPP)

System Address Maps

Memory Map

The first 640 KB of system board RAM is mapped starting at address 0000000h. A 256-byte area and a 1 KB area of this RAM are reserved for BIOS data areas. Memory can be mapped differently if POST detects an error. See the section about BIOS data areas in the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for details.

Figure 3. System Memory Map

Address Range (Decimal)	Address Range (Hex)	Size	Description
1024K–131072K	100000–8000000	127M	Extended memory
960K–1023K	F0000–FFFFF	64K	System BIOS
944K–959K	EC000–EFFFF	16K	Available
936K–943K	EA000–EBFFF	8K	ESCD (Plug and Play configuration area)
928K–935K	E8000-E9FFF	8K	Available
896K–927K	E0000–E7FFF	32K	BIOS reserved
800K–895K	C8000–DFFFF	96K	Available HI DOS memory (open to ISA and PCI bus)
640K–799K	A0000–C7FFF	160K	Video memory and BIOS
512K–639K	80000–9FFFF	128K	Extended
0K–511K	00000–7FFFF	512K	DOS applications (conventional)

Input/Output Address Map

The following figures list the system board I/O address maps. Any addresses that are not shown are reserved.

Figure 4 (Page 1 of 3). I/O Address Map

Address (Hex)	Device
0000–000F	DMA 1
0020–003F	Interrupt controller 1
0040–0043	Timer 1
0044–0047	Available I/O for ISA/PCI bus
0048–004B	Timer 2
004C–005F	Available I/O for ISA/PCI bus
0060	Keyboard controller data byte
0061	System Port B
0062–0063	Available I/O for ISA/PCI bus
0064	Keyboard controller, command and status byte
0065–006F	Available I/O for ISA/PCI bus
0070, bit 7	Enable/disable NMI
0070, bits 6:0	Real time clock address
0071	Real time clock data
0072–0077	Available I/O for ISA/PCI bus
0078	Reserved-system board setup
0079	Reserved-system board setup
007A–007F	Available I/O for ISA/PCI bus
0080	POST checkpoint register
0080-008F	DMA page register
0090–009F	Available I/O for ISA/PCI bus
00A0–00BF	Interrupt controller 2
00C0–00DE	DMA 2
00DF–00EF	Available I/O for ISA/PCI bus

Figure 4 (Page 2 of 3). I/O Address Map

Address (Hex)	Device
00F0	Coprocessor busy–Clear
00F1	Coprocessor reset
00F2–016F	Available I/O for ISA/PCI bus
0170–0177	IDE channel 1
01F0–01F7	IDE channel 0
01F8–021F	Available I/O for ISA/PCI bus
0220–0227	SMC FD-37C669, serial port 3 or 4
0228–0277	Available I/O for ISA/PCI bus
0278–027F	SMC FD-37C669, parallel port 3
0280–02E7	Available I/O for ISA/PCI bus
02E8–02EF	SMC FD-37C669, serial port 3 or 4
02F0–02F7	Available I/O for ISA/PCI bus
02F8–02FF	SMC FD-37C669, serial port 2 (system board)
0300–0337	Available I/O for ISA/PCI bus
0338–033F	SMC FD-37C669, serial port 3 or 4
0340–0375	Available I/O for ISA/PCI bus
0376–0377	IDE channel 1
0377, bit 7	IDE, diskette change
0378–037F	SMC FD-37C669, parallel port 2
0380–03B0	Available I/O for ISA/PCI bus
03BC–03BE	SMC FD-37C669, parallel port 1 (system board)
03E0–03E7	Available I/O for ISA/PCI bus
03E8–03EF	SMC FD-37C669, serial port 3 or 4
03F0–03F5	SMC FD-37C669, diskette channel 0
03F6	IDE channel 0
03F7, bit 7	IDE, diskette change
03F7, bits 6:0	IDE channel 0
03F8–03FF	SMC FD-37C669, serial port 1 (system board)
0400–0537	Available I/O for ISA/PCI bus
0CF8–0CFB	PCI configuration address register
0CFC–0CFF	PCI configuration data registers
0D00–0E7F	Available I/O for ISA/PCI bus
0E80–0E87	Available I/O for ISA/PCI bus
0E88–0F3F	Available I/O for ISA/PCI bus
0F40–0F47	Available I/O for ISA/PCI bus
0F47–042E7	Available I/O for ISA/PCI bus
42E8	Cirrus GD5436
42E9–4AE7	Available I/O for ISA/PCI bus
4AE8	Cirrus GD5436
4AE9–82E7	Available I/O for ISA/PCI bus
82E8	Cirrus GD5436
82E9–86E7	Available I/O for ISA/PCI bus
86E8	Cirrus GD5436
86E9–8AE7	Available I/O for ISA/PCI bus
8AE8	Cirrus GD5436
8AE9–8EE7	Available I/O for ISA/PCI bus
8EE8	Cirrus GD5436
8EE9–92E7	Available I/O for ISA/PCI bus
92E8	Cirrus GD5436
92E9–96E7	Available I/O for ISA/PCI bus
96E8	Cirrus GD5436
96E9–9AE7	Available I/O for ISA/PCI bus
9AE8	Cirrus GD5436
9AE9–9EE7	Available I/O for ISA/PCI bus
9EE8	Cirrus GD5436
9EE9–A2E7	Available I/O for ISA/PCI bus
A2E8	Cirrus GD5436
A2E9–A6E7	Available I/O for ISA/PCI bus
A6E8	Cirrus GD5436
A6E9–AAE7	Available I/O for ISA/PCI bus
AAE8	Cirrus GD5436
AAE9–B2E7	Available I/O for ISA/PCI bus
B2E8	Cirrus GD5436

Figure 4 (Page 3 of 3). I/O Address Map

Address (Hex)	Device
B2E9–B6E7	Available I/O for ISA/PCI bus
B6E8	Cirrus GD5436
B6E9–BAE7	Available I/O for ISA/PCI bus
BAE8	Cirrus GD5436
BAE9–BEE7	Available I/O for ISA/PCI bus
BEE8	Cirrus GD5436
BEE9–E2E7	Available I/O for ISA/PCI bus
E2E8	Cirrus GD5436
E2E9	Available I/O for ISA/PCI bus
E2EA	Cirrus GD5436
E2EB–FFFF	Available I/O for ISA/PCI bus

DMA I/O Address Map

Figure 5 (Page 1 of 2). DMA I/O Addresses for Memory Addresses, Word Counts, and Command/Status Registers

Address (hex)	Description	Bits	Byte Pointer
0000	Channel 0, Memory Address register	00–15	Yes
0001	Channel 0, Transfer Count register	00–15	Yes
0002	Channel 1, Memory Address register	00–15	Yes
0003	Channel 1, Transfer Count register	00–15	Yes
0004	Channel 2, Memory Address register	00–15	Yes
0005	Channel 2, Transfer Count register	00–15	Yes
0006	Channel 3, Memory Address register	00–15	Yes
0007	Channel 3, Transfer Count register	00–15	Yes
0008	Channels 0–3, Read Status/Write Command register	00–07	
0009	Channels 0–3, Write Request register	00–02	
000A	Channels 0–3, Write Single Mask register bits	00–02	
000B	Channels 0–3, Mode register (write)	00–07	
000C	Channels 0–3, Clear byte pointer (write)	N/A	
000D	Channels 0–3, Master clear (write)/temp (read)	00–07	
000E	Channels 0–3, Clear Mask register (write)	00–03	
000F	Channels 0–3, Write All Mask register bits	00–03	
0081	Channel 2, Page Table Address register[1]	00–07	
0082	Channel 3, Page Table Address register[1]	00–07	
0083	Channel 1, Page Table Address register[1]	00–07	
0087	Channel 0, Page Table Address register[1]	00–07	
0089	Channel 6, Page Table Address register[1]	00–07	
008A	Channel 7, Page Table Address register[1]	00–07	
008B	Channel 5, Page Table Address register[1]	00–07	
008F	Channel 4, Page Table Address/Refresh register	00–07	
00C0	Channel 4, Memory Address register	00–15	Yes
00C2	Channel 4, Transfer Count register	00–15	Yes
00C4	Channel 5, Memory Address register	00–15	Yes
00C6	Channel 5, Transfer Count register	00–15	Yes
00C8	Channel 6, Memory Address register	00–15	Yes
00CA	Channel 6, Transfer Count register	00–15	Yes
00CC	Channel 7, Memory Address register	00–15	Yes
00CE	Channel 7, Transfer Count register	00–15	Yes
00D0	Channels 4–7, Read Status/Write Command register	00–07	
00D2	Channels 4–7, Write Request register	00–02	
00D4	Channels 4–7, Write Single Mask register bit	00–02	
00D6	Channels 4–7, Mode register (write)	00–07	
00D8	Channels 4–7, Clear byte pointer (write)	N/A	
00DA	Channels 4–7, Master clear (write)/temp (read)	00–07	
00DC	Channels 4–7, Clear Mask register (write)	00–03	
00DE	Channels 4–7, Write All Mask register bits	00–03	

Figure 5 (Page 2 of 2). DMA I/O Addresses for Memory Addresses, Word Counts, and Command/Status Registers

Address (hex)	Description	Bits	Byte Pointer
00DF	Channels 5–7, 8- or 16-bit mode select	00–07	

[1] Upper byte of Memory Address register

IRQ and DMA Channel Assignments

The following figures list the interrupt request (IRQ) and direct memory access (DMA) channel assignments.

Interrupt Request Assignments (IRQ)

Figure 6. Interrupt Request Assignments

Interrupt Request (IRQ)	System Resource
NMI	Critical system error
SMI	System/power management interrupt
0	Reserved (internal timer)
1	Reserved (keyboard buffer full)
2	Reserved (cascade interrupt from slave)
3	Serial port 2[1]
4	Serial port 1[2]
5	Parallel port 2[1]
6	Diskette controller[2]
7	Parallel port 1[2]
8	Reserved (real-time clock)
9	Video adapter (if installed)[1]
10	ISA/PCI bus
11	ISA/PCI bus
12	Mouse port[1]
13	Reserved (math coprocessor)
14	IDE Channel 1[1]
15	IDE Channel 2[2]

[1] If not assigned, this resource is available for the ISA/PCI bus.
[2] If not assigned, this resource is available for the ISA bus.

DMA Channel Assignments

Figure 7. DMA Channel Assignments

DMA Channel	Data Width	System Resource
0	8 bits	ISA bus[1]
1	8 bits	ISA bus[1]
2	8 bits	Reserved (diskette drive)
3	8 bits	ECP/EPP parallel port[1]
4		Reserved (cascade channel)
5	16 bits	ISA bus
6	16 bits	ISA bus
7	16 bits	ISA bus

[1] If not assigned, this resource is available for the ISA bus.

Power Supply

The power supply converts the ac input voltage into four dc output voltages and provides power for the following:

- System board
- Adapters
- Internal DASD drives
- Keyboard and auxiliary devices

PC 100 and PC 300 computers have a 145-watt power supply. The following figure shows the input power specifications. The power available for each component within the system is shown in Figure 10 on page 12.

Figure 8. AC Input Power Requirements

Specification	Measurements
Input voltage (Range is switch selected; sine wave input is required.)	
Low range	110 (min)–127 (max) V ac
High range	200 (min)–240 (max) V ac
Input frequency	50 Hz ± 3 Hz or 60 Hz ± 3 Hz

Power Output Parameters

The power supply dc outputs shown in the following figure include the current supply capability of all the connectors including system board, DASD, PCI, and auxiliary outputs.

Figure 9. Power Output Parameters (145 Watt)

Output Voltage	Regulation	Minimum Current (amps)	Maximum Current (amps)
+5 volts	+5% to -4%	1.5 A	18.0 A
+12 volts	+5% to -4%	0.2 A	4.2 A
-12 volts	+10% to -9%	0.0 A	0.4 A
-5 volts	+5% to -4%	0.0 A	0.3 A

Component Outputs

The power supply provides separate voltage sources for the system board and internal storage devices. The following figure shows the approximate power that is provided for system components. Many components draw less current than the maximum shown.

Figure 10. Component Maximum Current

Supply Voltage (V dc)	Maximum Current (mA)	Regulation Limits
System Board:		
+5.0 V dc	4000 mA	+5.0% to –5.0%
+12.0 V dc	25.0 mA	+5.0% to –5.0%
–12.0 V dc	25.0 mA	+10.0% to –9.0%
Keyboard Port:		
+5.0 V dc	275 mA	+5.0% to –5.0%
Auxiliary-Device (Mouse) Port:		
+5.0 V dc	300 mA	+5.0% to –5.0%
AT-Bus Adapters (Per Slot):		
+5.0 V dc	4500 mA	+5.0% to –5.0%
–5.0 V dc	200 mA	+5.0% to –5.0%
+12.0 V dc	1500 mA	+5.0% to –5.0%
–12.0 V dc	300 mA	+5.0% to –5.0%
PCI-Bus Adapters (Per Slot)		
+5.0 V dc	5000 mA	+5.0% to –4.0%
Internal DASD:		
+5.0 V dc	1400 mA	+5.0% to –5.0%
+12.0 V dc	1500 mA	+5.0% to –5.0%

Note: Some adapters and hard disk drives draw more current than the recommended limits. These adapters and drives can be installed in the system; however, the power supply will shut down if the total power used exceeds the maximum power that is available.

Output Protection

The power supply protects against output overcurrent, overvoltage, and short circuits. Please see the power supply specifications for details.

A short circuit that is placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state, with no damage to the power supply.

If this shutdown state occurs, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least one second.

If an overvoltage fault occurs (in the power supply), the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of the nominal value of the power supply.

Connector Description

The power supply has four, 4-pin connectors for internal devices. The total power used by the connectors must not exceed the amount shown in Figure 10 on page 12. Signal and pin assignments are shown on page 20.

Physical Specifications

The following figure shows the physical specifications for the PC 100 and PC 300.

Figure 11. Physical Specifications

Size	
Width	440 mm (17.32 in.)
Depth	420 mm (16.53 in.)
Height	102 mm (4.00 in.)
Weight	
Minimum configuration	8.0 kg (17.61 lb)
Maximum configuration (fully populated with typical options)	10.0 kg (22.0 lb)
Cables	
Power cable	1.8 m (6 ft)
Keyboard cable	Approx. 2 m (10 ft)
Air Temperature	
System on	10.0 to 32.0°C (50 to 90°F)
System off	10.0 to 43.0°C (50 to 110°F)
Humidity	
System on	8% to 80%
System off	8% to 80%
Maximum Altitude[1]	2133.6 m (7000 ft)
Heat Output	
Minimum configuration	20 W (68.57 Btu per hour)
Maximum configuration[2]	210 W (719.25 Btu per hour)
Electrical	
Input voltage (range is switch selected; sine wave input is required)	
Low range	110 (min) to 127 (max) V ac
High range	200 (min) to 240 (max) V ac
Frequency	50 ± 3 Hz or 60 ± 3 Hz
Input, in kilovolt-ampere (kVA)	
Minimum configuration	0.08 kVA
Maximum configuration	0.30 kVA
Electromagnetic Compatibility	FCC Class B

[1] This is the maximum altitude at which the specified air temperatures apply. At higher altitudes, the maximum air temperatures are lower than those specified.
[2] Based on the 145-watt maximum capacity of the system power supply.

Advanced Power Management (APM)

The PC 100 and PC 300 come with built-in energy-saving capabilities. Advanced Power Management (APM) is a feature that reduces the power consumption of systems when they are not being used. APM, when enabled, initiates reduced-power modes for the monitor, microprocessor, and hard disk drive after a specified period of inactivity.

The following figure summarizes APM modes.

Figure 12. Advanced Power Management Modes

Mode	Power	Response
On (Ready)	System is at full power	Standard operation
On (Standby)	System is at reduced power	Any use of keyboard, mouse, or hard disk drive restores full power
Off	System is powered off	Power switch restores full power

The BIOS supports APM Version 1.2. This enables the system to enter a power-managed state, which reduces the power drawn from the ac wall outlet. Advanced Power Management is enabled through the Configuration/Setup Utility program and is controlled by the individual operating system.

Chapter 2. Connectors and Jumpers

System Board Connectors

The following figures show the connectors that are available on the system board and riser card.

Diskette Drive Connector

PC 100 and PC 300 computers have a 34-pin connector that supports the attachment of up to two diskette drives. The following figure shows the signal and pin assignments for the system board diskette drive connector.

Figure 13. Diskette Drive Connector Signal and Pin Assignments

Pin	Signal	Pin	Signal
1	Ground	2	High density select
3	Ground	4	Not connected
5	Ground	6	-Drive type
7	Ground	8	-Index
9	Ground	10	-Motor enable 0
11	Ground	12	-Drive select 1
13	Ground	14	-Drive select 0
15	Ground	16	-Motor enable 1
17	Ground	18	-Direction in
19	Ground	20	-Step
21	Ground	22	-Write data
23	Ground	24	-Write enable
25	Ground	26	-Track 0
27	Ground	28	-Write protect
29	n/c or key	30	-Read data
31	Ground	32	-Head 1 select
33	Ground	34	-Diskette change

Hard Disk Drive Connectors (Primary/Secondary)

PC 100 and PC 300 computers have two EIDE connectors for attaching IDE devices (such as hard disk drives and CD-ROM drives). The signals that are provided by these connectors include the 16-bit data bus, address lines A0 to A2, IRQ, and -IO CS16. These signals operate in the same way as the normal I/O-channel signals. The interface to the hard disk drive complies with *ANSI ATA-2 (AT Attachment).*

The address decode logic for the hard disk drive is on the system board. On a valid decode of A0 through A15 equal to 01F0h through 01F7h, -HFCS0 (0170h through 0177h, -HFCS2 for a secondary hard disk drive) goes active. On a valid decode of A0 through A15 equal to 03F6h through 03F7h, -HFCS1 (0376h through 0377h, -HFCS3 for a secondary hard disk drive) goes active.

The following figure shows the signal and pin assignments for the EIDE connectors.

Figure 14. EIDE Connector Signal and Pin Assignments

Pin	Signal	Pin	Signal
1	-RESET	2	Ground
3	Data bus bit 7	4	Data bus bit 8
5	Data bus bit 6	6	Data bus bit 9
7	Data bus bit 5	8	Data bus bit 10
9	Data bus bit 4	10	Data bus bit 11
11	Data bus bit 3	12	Data bus bit 12
13	Data bus bit 2	14	Data bus bit 13
15	Data bus bit 1	16	Data bus bit 14
17	Data bus bit 0	18	Data bus bit 15
19	Ground	20	Key (Reserved)
21	DRQ0/DRQ1	22	Ground
23	-IO Write	24	Ground
25	-IO Read	26	Ground
27	IO Channel Ready	28	VCC pullup
29	DACK0/DACK1	30	Ground
31	IRQ14/IRQ15	32	VCC pullup
33	Device address A1	34	Ground
35	Device address A0	36	Device address A2
37	-HFCS0	38	-HFCS1
39	Activity #	40	Ground

ISA Connectors

The I/O channel (ISA bus) is buffered to provide sufficient drive for the 98-pin connectors, assuming two low-power Schottky (LS) loads per slot.

The following figure shows the signal and pin assignments for the I/O channel connectors.

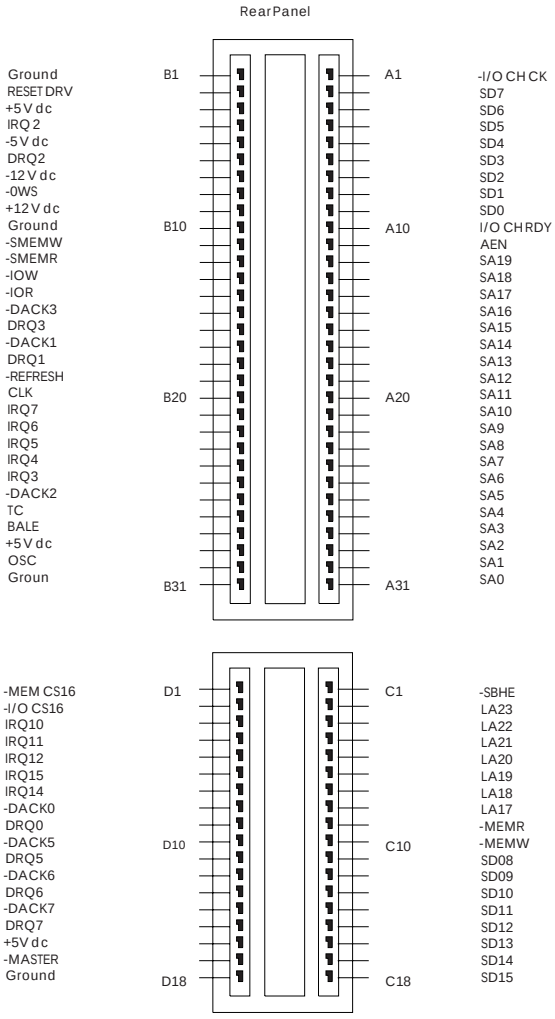


Figure 15. I/O Channel (ISA Bus) Connector

PCI Connectors

PC 100 and PC 300 computers have 124-pin peripheral component interconnect (PCI) connectors. Personal computers with PCI riser cards support the 32-bit, 5-V dc, local-bus signalling environment that is defined in the *PCI Local Bus Specification*. The following figure shows the signal and pin assignments for the PCI connectors.

Figure 16 (Page 1 of 2). PCI Connector Signal and Pin Assignments

Pin	Signal	Pin	Signal
1A	TRST#	1B	–12 V dc
2A	+12 V dc	2B	TCK
3A	TMS	3B	Ground
4A	TDI	4B	TDO
5A	+5 V dc	5B	+5 V dc
6A	INTA#	6B	+5 V dc
7A	INTC#	7B	INTB#
8A	+5 V dc	8B	INTD#
9A	Reserved	9B	PRSNT1#
10A	+5 V dc (I/O)	10B	Reserved
11A	Reserved	11B	PRSNT2
12A	Ground	12B	Ground
13A	Ground	13B	Ground
14A	Reserved	14B	Reserved
15A	RST#	15B	Ground
16A	+5 V dc (I/O)	16B	CLK
17A	GNT#	17B	Ground
18A	Ground	18B	REQ#
19A	Reserved	19B	+ 5 V dc (I/O)
20A	Address/Data 30	20B	Address/Data 31
21A	+3.3 V dc (not connected)[1]	21B	Address/Data 29
22A	Address/Data 28	22B	Ground
23A	Address/Data 26	23B	Address/Data 27
24A	Ground	24B	Address/Data 25
25A	Address/Data 24	25B	+3.3 V dc (not connected)[1]
26A	IDSEL	26B	C/BE 3“#
27A	+3.3 V dc (not connected)[1]	27B	Address/Data 23
28A	Address/Data 22	28B	Ground
29A	Address/Data 20	29B	Address/Data 21
30A	Ground	30B	Address/Data 19
31A	Address/Data 18	31B	+3.3 V dc (not connected)[1]
32A	Address 16	32B	Address/Data 17
33A	+3.3 V dc (not connected)[1]	33B	C/BE 2“#
34A	FRAME#	34B	Ground
35A	Ground	35B	IRDY#
36A	TRDY#	36B	+3.3 V dc (not connected)[1]
37A	Ground	37B	DEVSEL#
38A	STOP#	38B	Ground
39A	+3.3 V dc (not connected)[1]	39B	LOCK#
40A	SDONE	40B	PERR#
41A	SBO#	41B	+3.3 V dc (not connected)[1]
42A	Ground	42B	SERR#
43A	PAR	43B	+3.3 V dc (not connected)[1]
44A	Address/Data 15	44B	C/BE 1“#
45A	+3.3 V dc (not connected)[1]	45B	Address/Data 14
46A	Address/Data 13	46B	Ground
47A	Address/Data 11	47B	Address/Data 12
48A	Ground	48B	Address/Data 10
49A	Address/Data 9	49B	Ground
50A	Connector key	50B	Connector key
51A	Connector key	51B	Connector key
52A	C/BE 0“#	52B	Address/Data 8
53A	+3.3 V dc (not connected)[1]	53B	Address/Data 7
54A	Address/Data 6	54B	+3.3 V dc (not connected)[1]

Figure 16 (Page 2 of 2). PCI Connector Signal and Pin Assignments

Pin	Signal	Pin	Signal
55A	Address/Data 4	55B	Address/Data 5
56A	Ground	56B	Address/Data 3
57A	Address/Data 2	57B	Ground
58A	Address/Data 0	58B	Address/Data 1
59A	+5 V dc (I/O)	59B	+5 V dc (I/O)
60A	REQ64#	60B	ACK64#
61A	+5 V dc	61B	+5 V dc
62A	+5 V dc	62B	+5 V dc

[1] The 3.3-volt PCI bus pins are attached to a connector on the riser card that can be used as an input for 3.3 volts. The system does not provide this power.

Power Supply Connectors

The power supply utilizes 4-pin connectors for internal devices. The total power used by the connectors must not exceed the amount shown in Figure 10 on page 12.

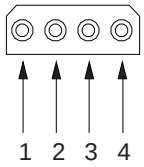


Figure 17. Power Supply Connector (Internal Devices) Signal and Pin Assignments

Pin	Signal	Pin	Signal
1	+12 V dc	3	Ground
2	Ground	4	+5 V dc

The following figure shows the signal and pin assignments for the system board 12-pin power supply connector.

Figure 18. Power Supply Connector (System Board) Signal and Pin Assignments

Pin	Signal	Pin	Signal
1	Power good (+5 V dc)	2	+5 V dc
3	+12 V dc	4	–12 V dc
5	Ground	6	Ground
7	Ground	8	Ground
9	–5 V dc	10	+5 V dc
11	+5 V dc	12	+5 V dc

System Board Memory Connectors

The following figure shows the signal and pin assignments for the 72-pin system board memory connectors. Data bits 0 through 15 are the low word, and data bits 16 through 31 are the high word.

Figure 19. System Board Memory Connector Signal and Pin Assignments

Pin	Signal	Pin	Signal
1	Ground	37	Parity 1 not used
2	Data 0	38	Parity 3 not used
3	Data 16	39	Ground
4	Data 1	40	Column address strobe 0
5	Data 17	41	Column address strobe 2
6	Data 2	42	Column address strobe 3
7	Data 18	43	Column address strobe 1
8	Data 3	44	Row address strobe 0
9	Data 19	45	Row address strobe 1
10	+5 V dc	46	Reserved
11	Reserved	47	Write enable
12	Address 0	48	Reserved
13	Address 1	49	Data 8
14	Address 2	50	Data 24
15	Address 3	51	Data 9
16	Address 4	52	Data 25
17	Address 5	53	Data 10
18	Address 6	54	Data 26
19	Address 10	55	Data 11
20	Data 4	56	Data 27
21	Data 20	57	Data 12
22	Data 5	58	Data 28
23	Data 21	59	+5 V dc
24	Data 6	60	Data 29
25	Data 22	61	Data 13
26	Data 7	62	Data 30
27	Data 23	63	Data 14
28	Address 7	64	Data 31
29	Reserved	65	Data 15
30	+5 V dc	66	Reserved
31	Address 8	67	Reserved
32	Address 9	68	Reserved
33	Row address strobe 3	69	Reserved
34	Row address strobe 2	70	Reserved
35	Parity 2 not used	71	Reserved
36	Parity 0 not used	72	Ground

Video Feature Connector

PC 100 and PC 300 computers have a 26-pin connector that supports the attachment of additional video features. The following figure shows the signal and pin assignments for the video feature connector.

Figure 20. Video Feature Connector

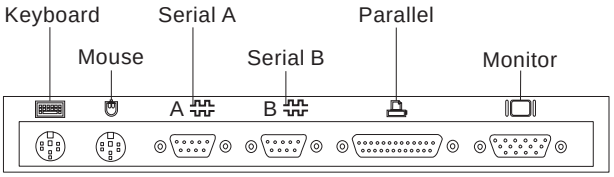
Pin	Signal	Pin	Signal
1	Ground	2	Data 0
3	Ground	4	Data 1
5	Ground	6	Data 2
7	Data enable	8	Data 3
9	Sync enable	10	Data 4
11	PCLK enable	12	Data 5
13	DDCCLK	14	Data 6
15	Ground	16	Data 7
17	Ground	18	PCLK
19	Ground	20	BLANK
21	Ground	22	HSYNC
23	VMCLK	24	VSYNC
25	DDC Data	26	Ground

I/O Connectors

The standard I/O device connectors include:

- A keyboard connector
- An auxiliary device (mouse) connector
- Two serial connectors
- A parallel connector
- A monitor connector

Each I/O connector on the back panel of the computer is identified by a symbol.



Keyboard and Auxiliary-Device (Mouse) Connectors

The keyboard and auxiliary-device (mouse) connectors use 6-pin, miniature DIN connectors.

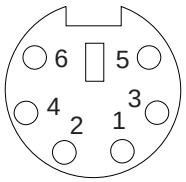


Figure 21. Keyboard Signal and Pin Assignments

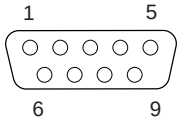
Pin	I/O	Signal Name
1	I/O	Data
2	NA	Aux data on keyboard connector
3	NA	Ground
4	NA	+5 V dc
5	I/O	Clock
6	NA	Aux clock on keyboard connector

Figure 22. Auxiliary-Device (Mouse) Signal and Pin Assignments

Pin	I/O	Signal Name
1	I/O	Data
2	NA	Reserved
3	NA	Ground
4	NA	+5 V dc
5	I/O	Clock
6	NA	Reserved

Serial Port Connectors

The two serial connectors on the back of the computer use a 9-pin, male, D-shell connector and pin assignments defined for RS-232D. The voltage levels are EIA only. Current loop interface is not supported.



The following figure shows the signal and pin assignments for the serial port connector in a communication environment.

Figure 23. Serial Port Connector Signal and Pin Assignments

Pin	I/O	Signal Name	Pin	I/O	Signal Name
1	I	Data carrier detect	6	I	Data set ready
2	I	Receive data	7	O	Request to send
3	O	Transmit data	8	I	Clear to send
4	O	Data terminal read	9	I	Ring indicator
5	NA	Signal ground			

Use Serial A or Serial B for high-speed modem and printer connections, or for devices such as a mouse or other pointing device.

The serial ports transfer data one bit at a time (serially) at speeds ranging from 300 to 345 600 bits per second (bps). The transfer rate is also referred to as *baud rate*. The serial ports on the computer are 16550-UART (universal asynchronous receiver/transmitter) compatible which means that they can support high-speed modems.

Serial-Port Setup

Each serial connector or adapter in the computer can use any of four available port settings, provided that a different setting is used for each. The settings include the port address (in hexadecimal) and the IRQ (interrupt request line), which determines how the microprocessor responds to an interrupt from the serial port. The four available port settings, in sequential order, are:

3F8h-IRQ 3 or 4
2F8h-IRQ 3 or 4
3E8h-IRQ 3 or 4
2E8h-IRQ 3 or 4

There is no direct relationship among the port connectors, the four available port settings, and the four COM numbers. When the computer is started, the power-on self-test (POST) assigns COM numbers to the port addresses that are actually in use at the time. POST goes down the list of addresses sequentially to assign COM numbers to each address in use by a serial device. If an address is not in use, a COM number is not assigned. POST assigns the next available COM number to the next address in use. The port addresses and IRQ for Serial A and Serial B are preset at the factory to:

Serial A: 3F8h-IRQ 4

Serial B: 2F8h-IRQ 3

POST assigns COM numbers to Serial A and Serial B during startup, as follows:

Serial A: 3F8h-IRQ 4 (COM1)

Serial B: 2F8h-IRQ 3 (COM2)

However, if the computer comes with an internal modem, the factory settings and COM assignments are:

Serial A: 3F8h-IRQ 4 (COM1)

Serial B: 2F8h-IRQ 3 (COM2)

Modem: 3E8h-IRQ 5 (COM3)

The port address and IRQ settings for Serial A and Serial B can be viewed using the Configuration/Setup Utility program. The COM numbers are not shown on the Configuration/Setup Utility program screens. However, you can use one of the diagnostic programs that comes with your computer to view them.

Parallel Port Connector

The parallel port connector is a standard 25-pin, D-shell connector. The following figure shows the signal and pin assignments for the parallel port connector.

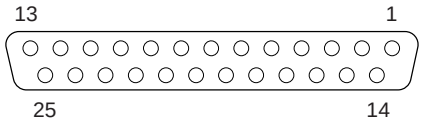


Figure 24. Parallel Port Connector Signal and Pin Assignments

Pin	I/O	Signal Name	Pin	I/O	Signal Name
1	O	-STROBE	14	O	-AUTO FD XT
2	I/O	Data bit 0	15	I	-ERROR
3	I/O	Data bit 1	16	O	-INIT
4	I/O	Data bit 2	17	O	-SLCT IN
5	I/O	Data bit 3	18	NA	Ground
6	I/O	Data bit 4	19	NA	Ground
7	I/O	Data bit 5	20	NA	Ground
8	I/O	Data bit 6	21	NA	Ground
9	I/O	Data bit 7	22	NA	Ground
10	I	-ACK	23	NA	Ground
11	I	BUSY	24	NA	Ground
12	I	PE	25	NA	Ground
13	I	SLCT			

The parallel port supports extended, high-speed modes, which means that it can transfer data up to 10 times as fast as a standard parallel port.

Parallel-Port Setup

Each parallel connector or adapter in your computer can use any of three available port settings, provided that a different setting is used for each. The settings include the port address (in hexadecimal) and the interrupt request line (IRQ), which determines how the microprocessor responds to an interrupt from the parallel port. The three available port settings, in sequential order, are:

3BCh-IRQ 5 or 7
378h-IRQ 5 or 7
278h-IRQ 5 or 7

There is no direct relationship among the three available port settings and the three LPT numbers. When you start the computer, POST (power-on self test) assigns LPT numbers to the port addresses that are actually in use at the time. POST goes down the list of addresses sequentially to assign LPT numbers to each address in use by a parallel device. If an address is not in use, an LPT number is not assigned to it. POST assigns the next available LPT number to the next address in use. The port address and IRQ setting for the built-in parallel port are preset at the factory, as follows:

Built-in port: 3BCh-IRQ 7

POST assigns an LPT number to the built-in parallel port during startup, as follows:

Built-in port: 3BCh-IRQ 7 (LPT1)

If you add another parallel adapter that uses the next sequential address, POST assigns LPT numbers as follows:

Built-in port: 3BCh-IRQ 7 (LPT1)

Adapter port: 378h-IRQ 5 (LPT2)

The port address and IRQ settings for the built-in parallel port can be viewed using the Configuration/Setup Utility program. The LPT number is not shown on the Configuration/Setup Utility program screens. However, you can use one of the diagnostic programs that comes with your computer to view it.

The parallel-port setting must be changed if you use ECP, EPP, or ECP/EPP modes because 3BCh-IRQ 7 cannot be used for these modes. The setting can be changed using the Configuration/Setup Utility program.

Parallel-Port Modes

The parallel port can operate in five different modes. One is a *standard,* unidirectional mode; the other four are *extended,* bidirectional modes that provide additional function and higher performance. Refer to the documentation that comes with your printer or other parallel device to determine the appropriate parallel mode to use and to get information on the required device drivers.

Standard This *AT-compatible mode* is the default mode. In this mode, the parallel port is limited to writing information to the device attached to it. This mode can be used with most IBM-compatible parallel printers.

Bidirectional This *PS/2-compatible mode* is a bidirectional mode used for data transfer to other PC systems and supported devices.

ECP The *extended capabilities port (ECP)* mode is a high-performance, bidirectional mode that uses direct memory access (DMA) for data transfer to a high-speed printer or to other devices.

EPP The *enhanced parallel port (EPP)* mode is a high-performance, bidirectional mode that has capabilities similar to the ECP mode. The main difference between the two modes is that EPP data transfers are processor-initiated instead of DMA-initiated. EPP supports the connection of up to eight external devices such as hard disk drives, CD-ROM drives, tape drives, diskette drives, and a printer to the parallel port. These devices can be connected to each other in a *daisy-chain* arrangement, or they can be connected through an external multiplexor. The attachment of multiple devices requires device drivers supplied by the device manufacturers.

ECP/EPP This mode combines the capabilities of the ECP and EPP modes. Select this mode to connect both ECP and EPP devices to the parallel port.

To select the mode of operation for the parallel port, use the Configuration/Setup Utility program.

Monitor Connector

PC 100 and PC 300 computers have a 15-pin monitor connector. The following figure shows the signal and pin assignments for the system board monitor connector.

Figure 25. Monitor Connector Signal and Pin Assignments

Pin	Signal	Pin	Signal
1	Red (out)	2	Green (out)
3	Blue (out)	4	Not used
5	Ground	6	Red ground
7	Green ground	8	Blue ground
9	Not used	10	Ground
11	Not used	12	DDC2 serial data (I/O)
13	Horizontal sync (out)	14	Vertical sync (out)
15	DDC2 clock (I/O)		

Chapter 3. Memory Subsystems

Memory-Module Description

PC 100 and PC 300 computers have four SIMM connectors. After memory modules are installed, the Plug and Play feature of the BIOS automatically detects the additional memory modules.

Notes:

1. Memory modules can have a maximum height of 1.2 inches.
2. Parity checking is not supported.
3. A mix of parity and non-parity SIMMs will be configured as non-parity.
4. A mix of extended-data output (EDO) and fast page (FP) SIMMs can be installed in the PC 300 if matched pairs are installed in each bank.

Memory-Module Configurations

The following tables show the typical memory-module configurations for the PC 100 and PC 300.

Figure 26. Memory-Module Type, Speed, and Size – PC 100

Type	Speed	Memory-Module Size
Fast page	70 ns	4 MB, 8 MB, 16 MB, 32 MB

Figure 27. Memory-Module Type, Speed, and Size – PC 300

Type	Speed	Memory-Module Size
EDO (preinstalled)	60 ns	4 MB, 8 MB, 16 MB, 32 MB
Fast page (supported)	70 ns	4 MB, 8 MB, 16 MB, 32 MB

Figure 28. System Memory Table

Total Memory	Bank 0 SIMM 1, 2	Bank 1 SIMM 3, 4
4 MB[1]	4, 0	0, 0
8 MB	4, 4	0, 0
16 MB	0, 0	8, 8
16 MB	4, 4	4, 4
24 MB	8, 8	4, 4
24 MB	4, 4	8, 8
32 MB	8, 8	0, 0
32 MB	0, 0	8, 8
40 MB	4, 4	16, 16
40 MB	16, 16	4, 4
48 MB	8, 8	16, 16
64 MB	16, 16	16, 16
64 MB	32, 32	0, 0
72 MB	4, 4	32, 32
80 MB	8, 8	32, 32
96 MB	16, 16	32, 32
128 MB	32, 32	32, 32

[1] A 4 MB, single SIMM is supported by the PC 100 only.

Cache Memory

Cache memory is a RAM storage location between the microprocessor and system memory. The microprocessor has a 16 KB, L1 (internal) cache. PC 100 and PC 300 computers also support up to 256 KB of L2 (external) cache. The following table shows the cache supported.

Figure 29. L1 and L2 Cache

L1 Cache Standard	L2 Cache Standard	L2 Cache Maximum
16 KB	0 KB	256 KB

Cache Upgrade Options

Use IBM option kit 76H0236 to upgrade L2 cache. The on-board L2 cache and tag ram sockets can be populated to a maximum of 256 KB. The cache design is direct-mapped (1-way associative) write-back, and the cache is unified (data and code). Refer to the following table for SRAM parameters.

Figure 30. Features of IBM Option Kit 76H0236

	SRAM	TAG
Size	32 K x 8	32 K x 8
Type	Asynchronous	Asynchronous
Voltage	3.3 v	5 v
Speed	15 ns	15 ns
Package	28-pin DIP (300 mil)	28-pin DIP (300 mil)
Quantity	8	1

Chapter 4. System Compatibility

Hardware Compatibility

This section briefly discusses hardware, software, and BIOS compatibility issues that must be considered when designing application programs.

Many of the interfaces are the same as those used by the IBM Personal Computer AT. In most cases, the command and status organization of these interfaces is maintained.

The functional interfaces are compatible with the following interfaces:

- The Intel 8259 interrupt controllers (edge-triggered mode).
- The National Semiconductor NS16450 and NS16550A serial communication controllers.
- The Motorola MC146818 Time of Day Clock command and status (CMOS reorganized).
- The Intel 8254 timer, driven from a 1.193 MHz clock (channels 0, 1, and 2).
- The Intel 8237 DMA controller, except for the Command and Request registers and the Rotate and Mask functions. The Mode register is partially supported.
- The Intel 8272 or 82077 diskette drive controllers.
- The Intel 8042 keyboard controller at addresses 0060h and 0064h.
- All video standards using VGA, EGA, CGA, MDA, and Hercules modes.
- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode.

Use the following information to develop application programs for personal computer products. Whenever possible, use the BIOS as an interface to hardware to provide maximum compatibility and portability of applications among systems.

Hardware Interrupts

Hardware interrupts are level sensitive for PCI interrupts and edge sensitive for ISA interrupts. The interrupt controller clears its in-service register bit when the interrupt routine sends an End-of-Interrupt (EOI) command to the controller. The EOI command is sent regardless of whether the incoming interrupt request to the controller is active or inactive.

The interrupt-in-progress latch is readable at an I/O-address bit position. This latch is read during the interrupt service routine and might be reset by the read operation, or it might require an explicit reset.

Note: For performance and latency considerations, designers might want to limit the number of devices sharing an interrupt level.

With level-sensitive interrupts, the interrupt controller requires that the interrupt request be inactive at the time the EOI command is sent; otherwise, a new interrupt request will be detected. To avoid this, a level-sensitive interrupt handler must clear the interrupt condition (usually by a read or write operation to an I/O port on the device causing the interrupt). After processing the interrupt, the interrupt handler:

1. Clears the interrupt
2. Waits one I/O delay
3. Sends the EOI
4. Waits one I/O delay
5. Enables the interrupt through the Set Interrupt Enable Flag command

Hardware interrupt IRQ9 is defined as the replacement interrupt level for the cascade level IRQ2. Program interrupt sharing is implemented on IRQ2, interrupt 0Ah. The following processing occurs to maintain compatibility with the IRQ2 used by IBM Personal Computer products:

1. A device drives the interrupt request active on IRQ2 of the channel.
2. This interrupt request is mapped in hardware to IRQ9 input on the second interrupt controller.
3. When the interrupt occurs, the system microprocessor passes control to the IRQ9 (interrupt 71h) interrupt handler.
4. This interrupt handler performs an EOI command to the second interrupt controller and passes control to the IRQ2 (interrupt 0Ah) interrupt handler.
5. This IRQ2 interrupt handler, when handling the interrupt, causes the device to reset the interrupt request before performing an EOI command to the master interrupt controller that finishes servicing the IRQ2 request.

Diskette Drives and Controller

The following figures show the reading, writing, and formatting capabilities of each type of diskette drive.

Figure 31. 5.25-Inch Diskette Drive Reading, Writing, and Formatting Capabilities

Diskette Drive Type	160/180 KB Mode	320/360 KB Mode	1.2 MB Mode
5.25-inch diskette drive:			
Single sided (48 TPI)	RWF	—	—
Double sided (48 TPI)	RWF	RWF	—
High capacity (1.2 MB)	RWF	RWF	RWF

R = Read W = Write F = Format

Figure 32. 3.5-Inch Diskette Drive Reading, Writing, and Formatting Capabilities

Diskette Drive Type	720 KB Mode	1.44 MB Mode
3.5-inch diskette drive:		
1.44 MB drive	RWF	RWF

R = Read W = Write F = Format

Notes:

1. Do not use 5.25-inch diskettes that are designed for the 1.2 MB mode in either a 160/180 KB or 320/360 KB diskette drive.
2. Low-density 5.25-inch diskettes that are written to or formatted by a high-capacity 1.2 MB diskette drive can be reliably read only by another 1.2 MB diskette drive.
3. Do not use 3.5-inch diskettes that are designed for the 2.88 MB mode in a 1.44 MB diskette drive.

Copy Protection

The following methods of copy protection might not work in systems using a 3.5-inch, 1.44 MB diskette drive.

- Bypassing BIOS routines:
  - Data transfer rate: BIOS selects the proper data transfer rate for the media being used.
  - Diskette parameter table: Copy protection, which creates its own diskette parameter table, might not work in these drives.
- Diskette drive controls:
  - Rotational speed: The time between two events in a diskette drive is a function of the controller.
  - Access time: Diskette BIOS routines must set the track-to-track access time for the different types of media that are used in the drives.
  - 'Diskette change' signal: Copy protection might not be able to reset this signal.
- Write-current control: Copy protection that uses write-current control does not work, because the controller selects the proper write current for the media that is being used.

Hard Disk Drives and Controller

Reading from and writing to the hard disk is initiated in the same way as in other IBM Personal Computer products; however, some new functions are supported.

Software Compatibility

To maintain software compatibility, the interrupt polling mechanism that is used by IBM Personal Computer products is retained. Software that interfaces with the reset port for the IBM Personal Computer positive-edge interrupt sharing (hex address 02F*x* or 06F*x*, where *x* is the interrupt level) does not create interference.

Software Interrupts

With the advent of software interrupt sharing, software interrupt routines must daisy chain interrupts. Each routine must check the function value, and if it is not in the range of function calls for that routine, it must transfer control to the next routine in the chain. Because software interrupts are initially pointed to address 0:0 before daisy chaining, check for this case. If the next routine is pointed to address 0:0 and the function call is out of range, the appropriate action is to set the carry flag and do a RET 2 to indicate an error condition.

Machine-Sensitive Programs

Programs can select machine-specific features, but they must first identify the machine and model type. IBM has defined methods for uniquely determining the specific machine type. The machine model byte can be found through Interrupt 15H, Return System Configuration Parameters function ((AH)=C0H). See the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for a listing of model bytes for other IBM Personal Computer products.

BIOS Compatibility

PC 100 computers support the following industry standard BIOS interfaces:

- Advanced Power Management (APM) Version 1.2
- Plug and Play (PnP) Version 1.0A
- Desktop Management Interface (DMI) Version 2.0

PC 300 computers support the following industry standard BIOS interfaces:

- Advanced Power Management (APM) Version 1.2
- Plug and Play (PnP) Version 1.0A

For additional information on BIOS interfaces supported, refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference*.

Chapter 5. Bus Architecture

Bus Architecture Descriptions

This section gives an overview of input/output (I/O) buses and explains how advanced I/O buses can improve performance.

A computer *bus* is a pathway of wires and signals that carry (or transfer) information inside the computer. *Information* includes data, addresses, instructions, and controls. The microprocessor has an external bus, called the *microprocessor bus* or *local bus*, that carries information between the microprocessor and main memory. The local bus has the same bus width (64 bits) as the microprocessor and operates at the same external speed.

Another computer bus, the *I/O bus* or *expansion bus*, carries information between the microprocessor or memory and the I/O (peripheral) devices. While microprocessor-bus performance has improved rapidly, improvements in I/O-bus performance have not equalled those of microprocessors and some peripheral devices, such as video and disk controllers. Regardless of how fast the microprocessor and other components are, data transfers between them must pass through the I/O bus.

The computer has two I/O buses: the *ISA bus* and the *PCI bus*. ISA has been the standard I/O bus used in IBM and IBM-compatible computers for many years. PCI is one of the advanced I/O bus standards developed by the computer industry to keep up with performance improvements of microprocessor buses and advanced peripheral devices. Although advanced designs, such as PCI, cannot match the performance of the microprocessor bus, they do achieve higher throughput by speeding up the I/O bus and widening its data path. PCI is intended to add to, but not replace, the capability of the ISA bus. In fact, most personal computers today need only three PCI connections: one for video, one for the disk controller, and one for a network adapter or other optional device.

ISA Bus

One of the most widely used and successful bus architectures is the AT bus, also called the *industry standard architecture (ISA) bus*, or the I/O channel. The ISA bus is a 16-bit bus that operates at a speed of 8 MHz. It can transfer up to 8 MB of data per second between the microprocessor and an I/O device. Practical performance ranges between 4 MB to 8 MB per second.

The ISA bus continues to be popular because so many adapters, devices, and applications have been designed and marketed for it. ISA is adequate for users of DOS applications in a stand-alone environment, or for DOS network requestors with moderate performance requirements.

Although the ISA bus is widely used and is suitable for many applications, it cannot transfer data fast enough for today's high-speed microprocessors and I/O devices. For example, the ISA bus might not provide for the performance needs of video devices and applications with high-resolution and high-color content. Also, ISA might not be capable of handling the throughput required by some fast hard disk drives, network controllers, or full-motion video adapters.

In PC 100 and PC 300 computers, the ISA bus is buffered to provide sufficient power for the 98-pin connectors, assuming two low-power Schottky (LS) loads per slot. The signal assignments and pin assignments for the I/O channel connectors are shown in Figure 15 on page 18.

PCI Bus

The PCI bus connects to the microprocessor local bus through a buffered bridge controller. A *bridge* translates signals from one bus architecture to another. PCI and ISA devices receive all their data and control information through the PCI controller. The PCI controller looks at all signals from the microprocessor local bus and then passes them to the ISA controller, or to peripheral devices connected to the PCI bus. However, the PCI bus is not governed by the speed of the microprocessor bus. PCI can operate at speeds as fast as 33 MHz, slow down, or even stop if there is no activity on the bus, all independent of the microprocessor's operations. This independence is a distinguishing feature of PCI that allows the microprocessor to do other work while the I/O bus is busy. Microprocessor independence also makes PCI adaptable to various microprocessor speeds and families and allows consistency in the design and use of PCI peripheral devices across multiple computer families.

PCI Performance

One of the most significant features of PCI is its 32-bit data path, which is twice the width of the ISA data path. With a 32-bit data path, the PCI bus can transfer more information per second than the ISA bus with its 16-bit data path. Also, PCI operates at higher speeds of up to 33 MHz. Depending on the mode of operation and computer components used, the PCI bus can transfer data at speeds up to 132 MB per second. While many factors can reduce practical performance, achieving just half or a third of the PCI maximum theoretical throughput far exceeds the practical performance of the ISA bus at 4 MB to 8 MB per second.

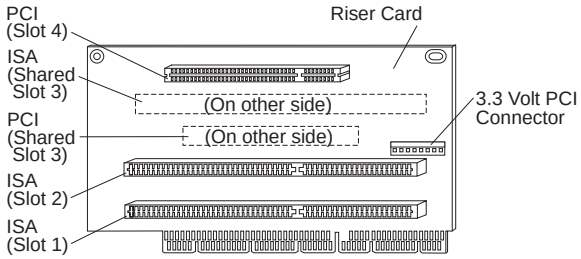
PCI Peripheral Devices

The wider data path and higher throughput make PCI a more suitable bus for today's high-speed microprocessors and I/O devices. Higher throughput translates into higher performance of peripheral devices, such as higher video resolutions, more colors, and quicker screen refreshes. The use of PCI architecture enhances the performance of the monitor and the storage devices. Both the video controller and the EIDE drive controller are connected to the PCI bus on the system board. Thus, the peripheral devices that have the greatest demand for high performance are supported by the benefits of PCI architecture.

Expansion-Bus Features

The bit-width of the I/O bus determines the type of adapters the computer supports. The shared slots handle 16-bit, ISA adapters and 32-bit, PCI adapters. The dedicated ISA slots handle 16-bit, ISA adapters only. The width of the I/O bus does not affect software compatibility.

The PC 100 and PC 300 riser card has one shared PCI and ISA slot, one dedicated PCI slot, and two dedicated ISA slots to support a maximum of four adapters at a given time.



One ISA connector and the PCI connector directly below it share an expansion-slot opening at the back of the computer that can be used by only one adapter at a time. This means that you can install either a PCI adapter or an ISA adapter in a shared slot, but not both.

PCI devices receive data through the PCI controller. The PCI controller looks at all signals from the microprocessor local bus, then passes them to the ISA controller or to peripherals connected to the PCI bus.

The signal assignments and pin assignments for the PCI connectors are shown in Figure 16 on page 19. For additional information, see the *PCI Local Bus Specification*, published by the PCI Special Interest Group.

Bus Voltage Levels

Four voltage levels are provided for I/O adapters. The maximum available values (for each slot) are as follows:

- +5 V dc (+5%, –4.5%) at 2.0 A
- –5 V dc (+10%, –9.5%) at 0.100 A
- +12 V dc (+5%, –4.5%) at 0.175 A
- –12 V dc (+10%, –9.5%) at 0.100 A

The I/O CH RDY signal is available on the I/O channel to allow operation with slow I/O or memory devices. I/O CH RDY is held inactive by an addressed device to lengthen the operation. For each clock cycle that the line is held inactive, one wait state is added to the I/O or DMA operation.

One voltage level is provided for PCI bus adapters. The maximum available values for each slot are +5 V dc (+5%, –4.5%) at 7.576 A.

Appendix A. Error Codes

This section identifies the POST error codes and beep error codes for the PC 100 and PC 300.

POST Error Codes

POST error messages appear when POST finds problems with the hardware during startup, or when a change in the hardware configuration is found. POST error messages are 3-, 4-, 5-, 8-, or 12-character alphanumeric messages. An *x* in an error message can represent any number.

Figure 33 (Page 1 of 2). POST Error Messages – PC 100 and PC 300

Code	Description
101	Interrupt failure
102	Timer failure
103	Timer-interrupt failure
104	Protected mode failure
105	Last 8042 command not accepted – keyboard failure
106	System board failure
108	Timer bus failure
109	Low MB chip select test
110	System board parity error 1 (system board parity latch set)
111	I/O parity error 2 (I/O channel check latch set)
112	I/O channel check error
113	I/O channel check error
114	External ROM checksum error
115	DMA error
116	System board port read/write error
120	Microprocessor test error
121	Hardware error
151	Real time clock failure
161	Bad CMOS battery
162	CMOS RAM checksum/configuration error
163	Clock not updating
164	CMOS RAM memory size does not match
167	Clock not updating
175	Riser card or system board error
176	System cover has been removed
177	Corrupted administrator password
178	Riser card or system board error
183	Administrator password has been set and must be entered
184	Password removed due to checksum error
185	Corrupted boot sequence
186	System board or hardware security error
189	More than three password attempts were made to access system
201	Memory date error
202	Memory address line error 00-15
203	Memory address line error 16-23
221	ROM to RAM remapping error
225	Unsupported memory type installed or memory pair mismatch
301	Keyboard error
302	Keyboard error
303	Keyboard to system board interface error
304	Keyboard clock high
305	No keyboard +5 V
601	Diskette drive or controller error
602	Diskette IPL boot record not valid
604	Unsupported diskette drive installed
605	POST cannot unlock diskette drive
662	Diskette drive configuration error
762	Math coprocessor configuration error

Figure 33 (Page 2 of 2). POST Error Messages – PC 100 and PC 300

Code	Description
11xx	Serial port error (xx = serial port number)
1762	Hard disk configuration error
1780	Hard disk 0 failed
1781	Hard disk 1 failed
1782	Hard disk 2 failed
1783	Hard disk 3 failed
1800	PCI adapter has requested an unavailable hardware interrupt
1801	PCI adapter has requested an unavailable memory resource
1802	PCI adapter has requested an unavailable I/O address space, or a defective adapter
1803	PCI adapter has requested an unavailable memory address space, or a defective adapter
1804	PCI adapter has requested unavailable memory addresses
1805	PCI adapter ROM error
1962	Boot sequence error
2401	System board video error
8601	System board - keyboard/pointing device error
8602	Pointing device error
8603	Pointing device or system board error
12092	Level 1 cache error (Processor chip)
12094	Level 2 cache error
16101	Riser card battery is dead
I9990301	Hard disk failure
I9990305	No operating system found

Beep Codes

For the following beep codes, the numbers indicate the sequence and number of beeps. For example, a "2-3-2" error symptom (a burst of two beeps, three beeps, then a burst of two beeps) indicates a memory module problem. An *x* in an error message can represent any number.

Figure 34. Beep Codes – PC 100

Beep Code	Probable Cause
1-2-2-3	BIOS ROM checksum
1-3-1-1	Test DRAM refresh
1-3-1-3	Keyboard controller
1-3-4-1	Memory Failure
1-3-4-3	Memory Failure
1-4-1-1	Memory Failure
2-1-2-3	ROM error
2-2-3-1	System board failure
1-2	Option card ROM failure

Figure 35. Beep Codes – PC 300

Beep Code	Probable Cause
1-1-3	CMOS write/read failure
1-1-4	BIOS ROM checksum failure
1-2-1	Programmable interval timer test failure
1-2-2	DMA initialization failure
1-2-3	DMA page register write/read test failure
1-2-4	RAM refresh verification failure
1-3-1	1st 64 K RAM test failure
1-3-2	1st 64 K RAM parity test failure
2-1-1	Slave DMA register test in progress or failure
2-1-2	Master DMA register test in progress or failure
2-1-3	Master interrupt mask register test failure
2-1-4	Slave interrupt mask register test failure
2-2-2	Keyboard controller test failure
2-3-2	Screen memory test in progress or failure
2-3-3	Screen retrace tests in progress or failure
3-1-1	Timer tick interrupt test failure
3-1-2	Interval timer channel 2 test failure
3-1-4	Time-of-Day clock test failure
3-2-4	Comparing CMOS memory size against actual
3-3-1	Memory size mismatch occurred

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